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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/566,221	09/20/2006	Hajime Nagai	1176/309	5690

46852 7590 11/13/2008

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EXAMINER	
TRAN, THIENVU V	
ART UNIT	PAPER NUMBER
2819	
MAIL DATE	DELIVERY MODE
11/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/566,221	NAGAI, HAJIME	
	Examiner	Art Unit	
	THIENVU V. TRAN	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 9-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2 and 9-24* is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/26/2006, 1/18/2008, 6/24/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Aoki et al (U.S. Patent No. 5,192,879).

With respect to claim 1, Aoki teaches a converting device comprising:

a first input portion receiving a first input signal (e.g., input_1) (see fig. 4 below);

a first output portion outputting a first output signal (e.g., output_1) (see fig. 4 below);

a second input portion receiving a second input signal (e.g., input_2) (see fig. 4 below);

a second output portion outputting a second output signal (e.g., output_2) (see fig. 4 below); and

a voltage dropping circuit (e.g., circuit containing transistors 2N, 2P, 1N, 1P) (see fig. 4) dropping voltages on a first node (e.g., node_1) (see fig. 4 below) located between said first input portion and said first output portion to ground voltage (e.g., when a low signal appears at the gate of transistors 2N and 2P, transistor 2P will turn on and 2N will turn off, thereby placing the node *node_1* at ground) (see fig. 4 below) and on a second node (e.g., node_2) (see fig. 4 below) located between said second input portion and said second output portion to ground voltage (e.g., when a high signal appears at the gate of transistors 1N and 1P, transistor 1N will turn on and 1P will turn off, thereby

placing the node *node_2* at ground) (see fig. 4 below), before changing from a state in which said first input portion is disconnected from said first node to a state in which said first input portion is connected to said first node (e.g., the node *node_1* is connected to the first input portion based on the control signal asserting and de-asserting transistor 2N/2P) (see fig. 4 below),

wherein in the state in which said input portion is connected to the first node, the first node and the second node are at complementary high and low voltages (e.g., when the input portion is connected to the first node, this would mean transistor 2N is turned on thereby allowing a connection between the input portion, e.g., portion that carries the first input, and the first node. The logic level on the first node would then be a logic one as indicated in figure 4 shown below. Inherent to the inverter configuration of 2N and 2P, the input to the inverter 2N/2P would be a logic zero as shown. The Applicant can trace backward the logic levels as shown in figure 4 below. As can clearly be seen, the logic levels at node 1 and node 2 are logic ones and logic zeros) (see fig. 4 below).

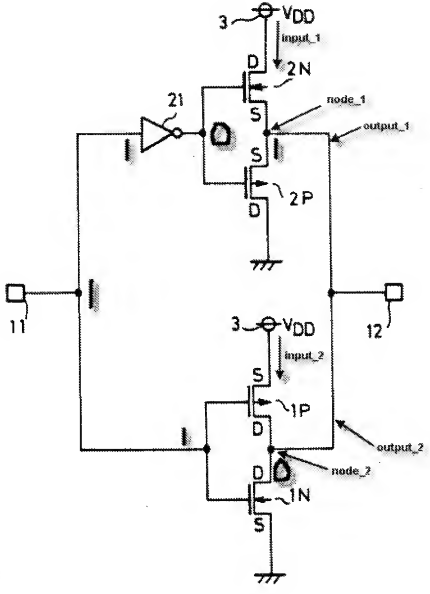
3
VDD
input_1
D
2N
21
node_1
S
output_1
S
2P
D
11
3
VDD
12
input_2
S
1P
D
output_2
node_2
D
1N
S

FIG. 4

Response to Arguments

3. Applicant's arguments filed 6/27/2008 have been fully considered but they are not persuasive.

With respect to claim 1, the Applicant argues the prior art reference Aoki does not teach the newly added limitation of "wherein in the state in which said input portion is connected to the first node, the first node and the second node are at complementary high and low voltages" (Applicant's Remarks, page 10). The Examiner respectfully disagrees. As pointed out in the detailed action above, the additional limitation is still being anticipated by Aoki. For example, when the input portion is connected to the first node, this would mean transistor 2N is turned on thereby allowing a connection between the input portion, e.g., portion that carries the first input, and the first node. The logic level on the first node would then be a logic one as indicated in figure 4 shown above. Inherent to the inverter configuration of 2N and 2P, the input to the inverter 2N/2P would be a logic zero as shown. The Applicant can trace backward the logic levels as shown in figure 4 above. As can clearly be seen, the logic level at node 1 and node 2 is a logic one and a logic zero.

Since the Examiner does not find the Applicant's argument persuasive with respect to claim 1, the rejection is therefore maintained.

Allowable Subject Matter

4. **Claims 2, 9-24** are allowed.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIENVU V. TRAN whose telephone number is (571)270-1276. The examiner can normally be reached on Monday-Friday (7:30AM-5:30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thienvu V Tran/

Examiner, Art Unit 2819

/Rexford N BARNIE/

Supervisory Patent Examiner, Art Unit 2819